A New "Active" Predistortor With High Gain Using Cascode-FET Structures

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Abstract — **An MMIC-compatible miniaturized "active" predistorter using cascode FET structures is presented. The predistorter has gain expansion and negative phase deviation characteristics required to compensate for the distortion of typical power amplifiers. Unlike the previously reported predistorters, the predistorter of this work is capable of providing gain as high as 7-17 dB, eliminating the need for additional buffer amplifiers. This makes our approach well suited to MMIC implementation. Analysis of gain and phase deviation was also conducted. From the analysis, the origin of nonlinear distortion of predistorter was found to be G_m of the upper FET and R_{ds} of the lower FET. The predistorter of this work was applied to linearize a 2-GHz MMIC power amplifier for CDMA handset applications. ACPR improvement of 5 dB was achieved.**

I. INTRODUCTION

High-efficiency and high-linearity MMIC power amplifier is a key component for handsets. To achieve high efficiency, the amplifiers are generally biased at class AB for low DC power consumption. However, this results in severe nonlinear distortions (both AM-AM and AM-PM). Among the two distortion mechanisms, phase distortion is hard to predict, and extensive research has been performed on the phase distortion of power amplifier [1]-[2].

Due to the distortions at high power levels, conventional PA's with low quiescent current are usually operated at reduced power levels (called power back-off) to satisfy the linearity requirement. However, the efficiency drops when an amplifier is operated under non-saturated conditions. In order to combat this problem, a linearizer is introduced so that the efficiency may not be compromised for linearity. The amount of power back-off can be reduced by employing the linearizers, resulting in enhanced efficiencies [3]-[4]. Among various linearization techniques, predistortion is the simplest to implement and can be realized in a small area, making it most compatible with MMIC implementation [5]-[6]. The reported predistorters were, however, "passive" and resulted in the insertion losses ranging from several dB to more than 10dB. Buffer amplifier is thus needed after the predistorter to compensate for the gain loss, which makes the predistortion system complicated and less suited to MMIC amplifiers.

In this work, a new "active" predistorter is proposed using a cascode FET structures. A simple analysis on the phase characteristics is also given in this work. The proposed predistorter allows gain while compensating for both gain and phase distortion. The need for additional buffer amplifiers is eliminated in this way. Moreover, it can eventually replace the driver stage of the PA, resulting in a small chip size.

II. OPERATION PRINCIPLE

Typically, power amplifier shows gain compression and positive phase deviation at high power levels. The predistorter is thus required to present positive gain and negative phase slopes at high power levels. Fig. 1 is the configuration of predistorter proposed in this work. It consists of two FET's connected in a cascode configuration, and bias inductors and resistors. It is simple and can be implemented easily in MMIC forms. Due to

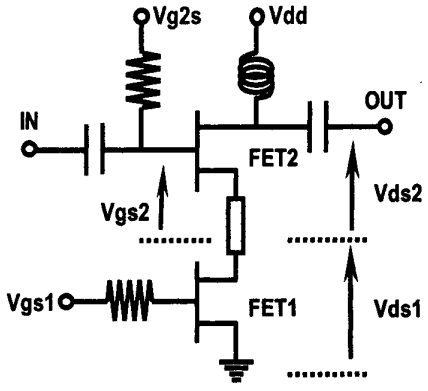

Fig. 1 Schematic diagram of predistorter

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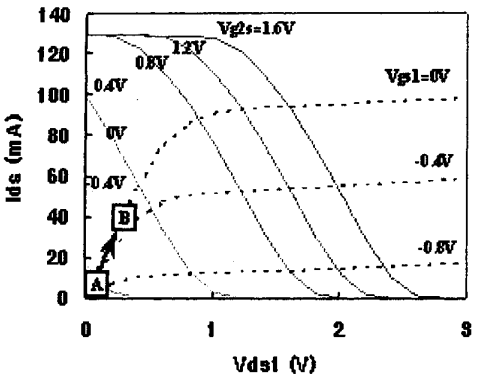


Fig. 2 Effective bias shift in DC-IV of predistorter

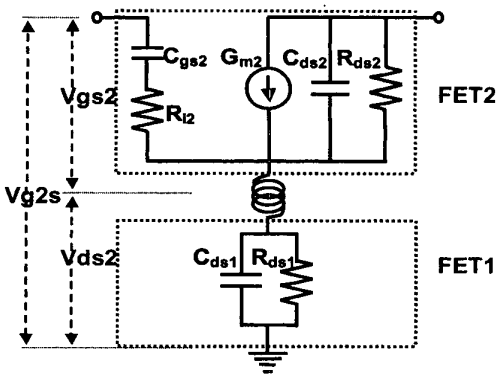


Fig. 3 Equivalent circuit model for predistorter

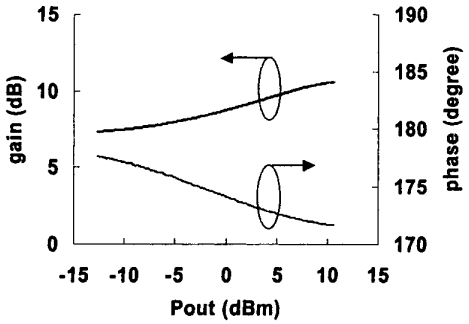


Fig. 4 Measured gain and phase

the fact that cascode-connected FETs use the same current path, and V_{dd} voltage is divided between the two FET's, it is possible to change the effective bias point of the FET with the input power levels as shown in Fig. 2.

Fig. 2 is the IV curve at each V_{gs1} and V_{g2s} bias voltage. A-region is selected as the stand-by bias point in this work. The stand-by current is very small, resulting in negligible DC power consumption. As the input RF power is increased, the DC component of the rectified current increases because the current is clipped at the lower side. So, the effective bias point shifts to a higher current region (B-region) at high power levels. Since the effective bias current to the FET2 is increased, the gain becomes higher, resulting in positive gain slope.

III. ANALYSIS AND MEASURED RESULTS

Unlike the gain characteristics, it is hard to predict and understand the phase variation. So, a simple analysis was conducted on the phase characteristics. Fig. 3 is the equivalent circuit of the predistorter. The lower FET is represented by a parallel combination of a resistor and a capacitor while the upper one is represented by the full equivalent circuit.

The analysis procedure can be summarized as follows. First, a table-based nonlinear transistor model was extracted from measured multiple-bias S-parameter data. Single-tone harmonic balance analysis was followed at various input power levels to determine the instantaneous time-domain voltage waveforms. Given the voltage waveforms, harmonic frequency components of each nonlinear parameter are identified by Fourier Transforms. Using the fundamental frequency components, we can derive the two-port S-parameters at each input power level. Gain (AM-AM) and phase variation (AM-PM) can then be evaluated as a function of the input power. The analysis is valid only when the input power is not excessive and higher-order effects are minor. However, the analysis is simple and allows one to identify the main sources of AM-AM and AM-PM variation.

The simple analysis showed that G_m of the upper FET (G_{m2}) and R_{ds} of lower FET (R_{ds1}) are most responsible for gain and phase variation in the cascode structure.

Cascode FET predistorter has been realized in an MMIC form using AlGaAs/InGaAs PHEMT's. Fig. 4 shows the measured gain and phase of predistorter as a function of the output power levels. Small signal gain as high as 7dB was obtained together with the required gain and phase predistortion characteristics for linearization of typical power amplifiers.

Another advantage of the predistorter of this work is the ability to control the gain and phase variation characteristics by changing V_{g2s} (gate bias to common-gate FET). Depending on V_{g2s}, gain and phase expansion characteristics can be tuned as shown in Fig. 5. One can change the power range of gain overshoot and phase undershoot by mere bias control of V_{g2s}.

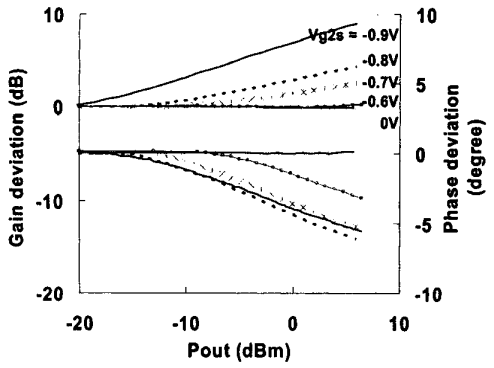


Fig. 5 Measured gain and phase deviation as a function of V_{g2s} control voltage

It is also worthwhile to note that the overall gain of the predistorter can be controlled by V_{g2s}. Depending on Vg2s, it can be as high as 17dB, which is much greater than the previously reported results showing losses [3]-[4]. The cascode-based predistorter can in this way be used as a driver amplifier. The need for additional buffer amplifiers is thus eliminated. These features facilitate monolithic integration of predistorters with power amplifiers in a small chip.

IV. APPLICATION TO LINEARIZED POWER AMPLIFIER

A 3-stage MMIC power amplifier (PA) integrated with the predistorter of this work was designed and fabricated for CDMA applications at 2GHz. A commercial GaAs PHEMT foundry was used for fabrication. The fabricated MMIC power amplifier is shown in Fig. 6. For reducing chip size, the output matching was done outside the chip. Total gate width is 4.8mm for power stage and 0.6mm for driver stage. The amplifier was biased at class-AB. The power amplifier has a linear gain of 33dB and single-tone saturated output power of 29.5dBm at 2GHz.

Fig. 7(a) shows the gain and phase deviation of the linearized PA. Even though gain overshoot became more pronounced over the mid power range, P_{1dB} was increased by using a predistorter. Phase deviation was also reduced to less than 2° for the input power levels all the way up to P_{1dB} compression point.

Fig. 7(b) shows measured ACPR of the linearized PA using O-QPSK CDMA modulated signals. Due to the compensated AM-AM and AM-PM characteristics, ACPR was improved by 3dB at an output power level of 23.5dBm and 5dB at 20.5dBm output power.

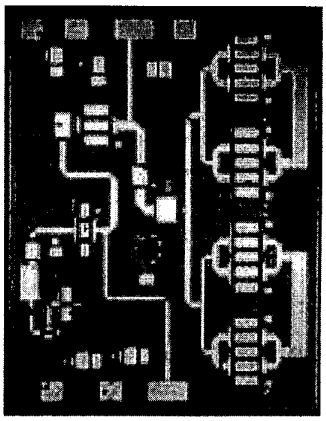
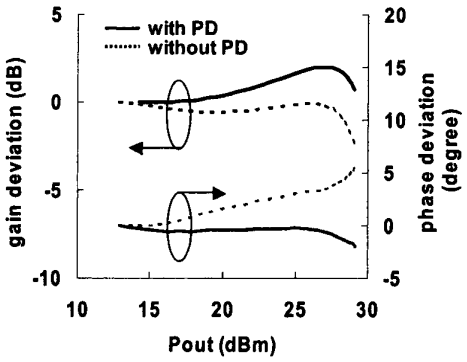
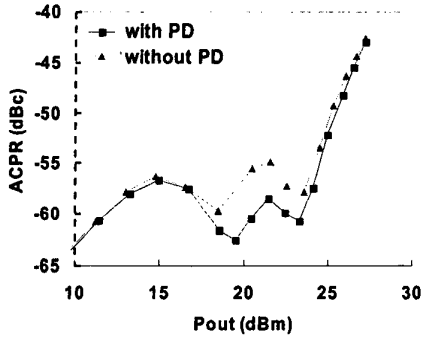


Fig. 6 Photograph of MMIC power amplifier



(a)



(b)

Fig. 7 Measured characteristics of PA with and without PD at 2GHz.
(a) Single-tone gain and phase deviation (b) ACPR

V. CONCLUSIONS

A high-gain predistorter using cascode HEMT structure has been developed. It shows appropriate gain expansion and negative phase deviation characteristics to linearize typical GaAs PA's, as well as high gain. The need for buffer amplifier is thus eliminated, making this approach well suited to MMIC implementation. Predistorter was analyzed using a simple equivalent circuit. From the analysis, nonlinear sources of gain and phase deviation were found to be G_{m2} and R_{ds1}.

Predistorter was integrated with a 2-GHz CDMA MMIC power amplifier. It showed ACPR improvement as much as 5 dB for OQPSK signals.

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